REMARKS

The Examiner objected to claims 24, 30 and 34. Applicants assert the Examiners objection to claims 24 and 34 are moot in light of Applicants canceling claims 24 and 34. Applicants assert the Examiners objection to claim 30 is moot in light of Applicants amending claim 30.

The Examiner rejected claims 30 and 34 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner rejected claims 1, 4, 6-8, 13, 15-16, 30-31 and 34-36 under 35 U.S.C. § 102(b) as allegedly being anticipated by Banerjee (U.S. Pat. 6,566,757).

The Examiner rejected claims 1, 8, 17 and 32 under 35 U.S.C. § 102(b) as allegedly being anticipated by Yabu (U.S. Pat. 5,989,992).

The Examiner rejected claims 2 and 9 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Banerjee (U.S. Pat. 6,566,757) in view of Shroff (U.S. Pat. 6,500,750).

The Examiner rejected claims 5 and 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Banerjee (U.S. Pat. 6,566,757) in view of Bohr (U.S. Pub. 2002/0064929).

The Examiner rejected claims 3 and 10 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yabu (U.S. Pat. 5,989,992).

The Examiner rejected claims 11-12 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yabu (U.S. Pat. 5,989,992) in view of Bohr (U.S. Pub. 2002/0064929).

Applicants respectfully traverse the §112 (2nd paragraph), §102(b) and §103(a) rejections with the following arguments.

35 USC § 112 Rejection, Second Paragraph

The Examiner rejected claims 30 and 34 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants believe the amendment of claim 30 overcomes the Examiners rejection of claim 30. Applicants have distinguished between the initial "top surfaces of the first and second dielectric layers" and "newly formed top surfaces of the first and second dielectric layers" after a "removing" step. The Examiner isinvited view Applicants FIGs 6D, 6E and 6H to see how it is possible for "said newly formed top surface (266) of said first dielectric layer completely surrounds said newly formed top surface (267) of said second dielectric layer."

Applicants assert, the Examiners rejection of claim 34 is moot in light of Applicants canceling claim 34.

35 USC § 102 Rejections

The Examiner rejected claims 1, 4, 6-8, 13, 15-16, 30-31 and 34-36 under 35 U.S.C. § 102(b) as allegedly being anticipated by Banerjee (U.S. Pat. 6,566,757).

The Examiner stated: "Banerjee [Figs. 5-7] discloses a method, comprising: providing a substrate [102]; forming a passivation layer on a top surface of said substrate [Col. 4 lines 42-48]; forming an electrically conductive layer [104] on a top surface of said substrate; passivation layer; patterning said conductive layer into a plurality of wire bond pads spaced apart; top surfaces of said wire bond pads coplanar after said patterning; said top surface of said substrate exposed between said wire bond pads, top surfaces of said wire bond pads being top surfaces of said conductive layer; a top surface of said conductive layer and top surfaces of said wire bond pads being a same surface, said top surfaces being parallel to said top surface of said substrate [Col. 4 lines 42-48]; after said patterning; after said step (d); (e) forming a dielectric layer [103,107,108] directly on said top surface of said substrate; said passivation layer; in spaces between adjacent wire bond pads and directly on said top surfaces of said wirebond pads; said dielectric layer filling said spaces; and after said forming said dielectric layer; after step (e); (f) completely removing said dielectric layer [103,107,108] from said top surfaces of said conductive layer of said wirebond pads, top surfaces of said dielectric layer in said spaces coplanar with said top surfaces of said wire bond pads [Fig. 6]."

First, Applicants point out that in Banerjee FIGs. 5, 6 and 7, the structures labeled 104 cannot be wire bond pads because in FIG. 7 a metal layer 112 is formed on top of dielectric layer 112 and vias 110 short all structures 104 together. Besides being shorted together, being covered by metal layer 112 makes it impossible to use structures 104 as wire bond pads.

Second, Applicants respectfully contend that Banerjee does not anticipate claim 1, as amended, because Banerjee does not teach each and every feature of claim 1.

In a first example, Banerjee does not teach: "forming a plurality of electrically conductive wires in said interlevel dielectric layer, top surfaces of said wires coplanar with a top surface of said interlevel dielectric layer." Banerjee specifically teaches in col. 4, lines 9-13 that there are no metal layers under layer 104. Further, there is no teaching as to the structural limitations of "top surfaces of said wires coplanar with a top surface of said interlevel dielectric layer."

In a second example, Banerjee does not teach: "forming a passivation layer on said top surfaces of said wires and said interlevel dielectric layer." There is no passivation layer or dielectric layer under layer 104 of Banerjee.

In a third example, Banerjee does not teach: "removing regions of said passivation layer to form via opening in said passivation layer over said plurality of wires, there being a respective via opening for each wire of said plurality of wires, said via openings extending from a top surface of said passivation layer to said top surfaces of said wires." There is no teaching of vias between structures 104 and wires under structure 104 in Banerjee.

In a fourth example, Banerjee does not teach: "after said forming said first dielectric layer, forming a second dielectric layer on a top surface of said first dielectric layer, said second dielectric layer filling remaining spaces between adjacent sidewalls of said wire bond pads." In Banerjee FIG. 5, second layer 107 does not fill the remaining spaces between structures 104, it requires a third layer 108 to do so. If 107 did fill those spaces, the structure of FIG. 6 where layer 108 caps layer 107 would not be possible.

In a fifth example, Banerjee does not teach: "after said forming said second dielectric layer, completely removing said first and second dielectric layers from said top surfaces of said wire bond pads, newly formed top surfaces of said first and second dielectric layers coplanar

with said top surfaces of said wire bond pads." In Banerjee FIG. 6, third layer 108 is coplanar with layer 104, not with second layer 107.

Based on the preceding arguments, Applicants respectfully maintain that Banerjee does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 2-7, 30-32 and 37-39 depend from claim 1, Applicants contend that claims 2-7, 30-32 and 37-39 are likewise in condition for allowance.

As to claim 4, Applicants would point out that Banerjee does not teach "said final dielectric layer extending over said first and second ends of said wire bond pads and over said via openings" as Applicants claim 4 requires. In Banerjee FIGs. 5, 6 and 7, there are no via opening under layer 103/107/108 for layers 103/107/108 to extend over. Applicants contend claim 4 is allowable.

As to claim 30, Applicants would point out that it can not be ascertained that first layer the top surface of first layer 103 "completely surrounds" the top layer of second layer 107 (as Applicants claim 30 requires) from Banerjee FIGs. 5, 6 and 7 as there is only one section view. Two sections views and/or a top view would be required, as Applicants have supplied in Applicants FIGs. 3, 4 and 5. Applicants contend claim 30 is allowable.

As to claim 31, Applicants would point out there is no teaching of wires under Banerjee layer 104, so there can be no "plurality of electrically conductive wires" no less the specific method of forming then as in Applicants claim 31. Applicants contend claim 30 is allowable.

Applicants respectfully contend that 35 USC § 102(b) rejection of 8, 15-16, and 34-36 based on Banerjee are moot in light of Applicants canceling claims 8, 15-16, and 34-36.

The Examiner rejected claims 1, 8, 17 and 32 under 35 U.S.C. § 102(b) as allegedly being anticipated by Yabu (U.S. Pat. 5,989,992).

The Examiner stated: "Yabu [Figs. 16-17] discloses a method, comprising: providing a substrate [Col. 6 line 66 – col. 7 line 12]; forming a passivation layer [Inherent] on a top surface of said substrate [Col. 6 line 66 – col. 7 line 12]; forming an electrically conductive layer [12] on a top surface of said substrate; passivation layer; patterning said conductive layer into a plurality of wire bond pads spaced apart; top surfaces of said wire bond pads coplanar after said patterning; said top surface of said substrate exposed between said wire bond pads, top surfaces of said wire bond pads being top surfaces of said conductive layer; a top surface of said conductive layer and top surfaces of said wire bond pads being a same surface, said top surfaces being parallel to said top surface of said substrate [Fig. 17(a)]; after said patterning; after said step (d); (e) forming a dielectric layer [13] directly on said top surface of said substrate; said passivation layer; in spaces between adjacent wire bond pads and directly on said top surfaces of said wire bond pads; said dielectric layer filling said spaces [Co1. 17 lines 45-48]; and after said forming said dielectric layer; after step (e); (f) completely removing said dielectric layer [13] from said top surfaces of said conductive layer of said wire bond pads, top surfaces of said dielectric layer in said spaces coplanar with said top surfaces of said wire bond pads [Fig. 17(b)].

Applicants respectfully contend that Yabu does not anticipate claim 1, as amended, because Yabu does not teach each and every feature of claim 1.

In a first example, Yabu does not teach: "forming a plurality of electrically conductive wires in said interlevel dielectric layer, top surfaces of said wires coplanar with a top surface of said interlevel dielectric layer." The Examiner indicated metal layers under layer 20 of Yabu FIG. 16 were "inherent." Applicants point out that in Yabu col. 6, line 66 to col. 7, line 12, Yabu simply indicates that the existence of metal layers is inherent. The Examiner has not shown that

the structural limitations of "top surfaces of said wires coplanar with a top surface of said interlevel dielectric layer" as required by Applicants claim 1 is inherent in Yabu.

In a second example, Yabu does not teach: "forming a passivation layer on said top surfaces of said wires and said interlevel dielectric layer." There is no passivation layer or dielectric layer under layer 104 of Yabu. The Examiner indicated a passivation layer under layer 20 of Yabu FIG. 16 was "inherent." Applicants point out that in Yabu col. 6, line 66 to col. 7, line 12, Yabu simply indicates that the existence of a dielectric layers (not passivation layers) is inherent. Even assuming if the existence of a passivation layer was taught, the Examiner has not shown that any passivation layer of Yabu is inherently "on said top surfaces of said wires and said interlevel dielectric layer" as Applicants claim 1 requires.

In a third example, Yabu does not teach: "removing regions of said passivation layer to form via opening in said passivation layer over said plurality of wires, there being a respective via opening for each wire of said plurality of wires, said via openings extending from a top surface of said passivation layer to said top surfaces of said wires." There is no teaching of vias between structures 12 and wires under structure 12 in Yabu no less "a respective via opening for each wire" as Applicants claim 1 requires.

In a fourth example, Yabu does not teach: "after said forming said first dielectric layer, forming a second dielectric layer on a top surface of said first dielectric layer, said second dielectric layer filling remaining spaces between adjacent sidewalls of said wire bond pads." In Yabu FIGs. 16, and 17a-17c, only a single dielectric layer 13 is taught.

In a fifth example, Yabu does not teach; "said first dielectric layer not filling said spaces between adjacent sides of said wire bond pads." Applicants point out, dielectric layer 13 fills the space between wires 12 in Yabu FIGs. 16 and 17a-17c.

In a sixth example, Yabu does not teach: "after said forming said second dielectric layer, completely removing said first and second dielectric layers from said top surfaces of said wire bond pads, newly formed top surfaces of said first and second dielectric layers coplanar with said top surfaces of said wire bond pads." In Yabu FIG. 17b, only single layer 13 is coplanar with wires 12.

Based on the preceding arguments, Applicants respectfully maintain that Yabu does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 2-7, 30-32 and 37-39 depend from claim 1, Applicants contend that claims 2-7, 30-32 and 37-39 are likewise in condition for allowance.

Applicants respectfully contend that 35 USC § 102(b) rejections of 8, 15-16, and 34-36 based on Yabu are moot in light of Applicants canceling claims 8, 15-16, and 34-36.

35 USC § 103 Rejections

The Examiner rejected claims 2 and 9 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Banerjee (U.S. Pat. 6,566,757) in view of Shroff (U.S. Pat. 6,500,750).

As to claim 2, Applicants have argued *supra* in response to the Examiners § 102(b) rejection of claim 1 that claim 1 is allowable, since claim 2 depends from claim 1, Applicants respectfully maintain that claim 2 is not unpatentable over Banerjee in view of Shroff and is in condition for allowance. Claim 9 has been canceled.

The Examiner rejected claims 5 and 14 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Banerjee (U.S. Pat. 6,566,757) in view of Bohr (U.S. Pub. 2002/0064929).

As to claim 5, Applicants have argued *supra* in response to the Examiners § 102(b) rejection of claim 1 that claim 1 is allowable, since claim 5 depends from claim 1, Applicants respectfully maintain that claim 5 is not unpatentable over Banerjee in view of Bohr and is in condition for allowance. Claim 14 has been canceled.

The Examiner rejected claims 3 and 10 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yabu (U.S. Pat. 5,989,992).

As to claim 3, Applicants have argued *supra* in response to the Examiners § 102(b) rejection of claim 1 that claim 1 is allowable, since claim 3 depends from claim 1, Applicants respectfully maintain that claim 3 is not unpatentable over Yabu and is in condition for allowance. Claim 10 has been canceled.

Applicants further point out that in rejecting claim 1, the Examiner indicated structures 12 were the bonding pads. In rejecting claim 3, the Examiner indicated structures 15 were the bonding pads. The Examiner cannot designate two different elements of the same reference as

representing the same element in two different claims. Applicants contend the 35 U.S.C. § 103(a) rejection of claim 3 based on Yabu is improper and request it be withdrawn.

The Examiner rejected claims 11-12 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yabu (U.S. Pat. 5,989,992) in view of Bohr (U.S. Pub. 2002/0064929). Applicants assert the 35 U.S.C. § 103(a) of claims 11 and 12 are moot in light of Applicants canceling claims 11 and 12.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Daubenspeck et al.

Dated: 10/6/07

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